CLAIMS

What is claimed is:

1. A method, comprising:

determining a reference resistance of a reference wafer;

determining a calibration resistance of a calibration wafer;

comparing the reference resistance with the calibration resistance; and

selecting an error trigger value based on the comparing of reference resistance with the calibration resistance.

2. The method of claim 1, wherein determining a reference resistance comprises:

measuring a first electrochemical deposition cell voltage of the reference wafer; and

calculating the reference resistance using the first electrochemical deposition cell voltage of the reference wafer.

3. The method of claim 2, further comprising measuring a first plurality of electrochemical deposition cell voltages of the reference wafer at a corresponding first plurality of electrochemical deposition currents.

4. The method of claim 2, wherein determining a calibration resistance comprises:

measuring a second electrochemical deposition cell voltage of the calibration wafer; and

calculating the calibration resistance using the second electrochemical deposition cell voltage of the calibration wafer.

5. The method of claim 2, further comprising measuring a second plurality of electrochemical deposition cell voltages of the calibration wafer at a corresponding second plurality of electrochemical deposition currents.

6. The method of claim 1, further comprising monitoring a electrochemical deposition of one or more production wafers using the selecting error trigger value.

7. The method of claim 6, wherein monitoring further comprises:

measuring the electrochemical deposition cell voltages of the one or more production wafers; and

determining when one of the electrochemical deposition cell voltages of the one or more production wafers is approximately equal to or greater than the edge trigger value.

8. The method of claim 7, further comprising aborting the electrochemical deposition of the one or more production wafers when the one of the electrochemical deposition cell voltages of the one or more production wafers is determined to be approximately equal to or greater than the edge trigger value.

9. The method of claim 7, wherein the error trigger value is selected to be approximately a 25% difference from a measured first electrochemical deposition cell voltage of the reference wafer.

10. The method of claim 1, wherein the reference wafer has a conducting layer disposed over a non-conducting layer, the non-conducting layer is substantially covered with the conducting layer at an edge of the reference wafer, and wherein the calibration wafer has a conducting layer disposed over a non-conducting layer, the non-conducting layer of the calibration wafer is substantially uncovered by the conducting layer of the calibration wafer at an edge of the calibration wafer

11. The method of claim 10, wherein the conducting layers of the calibration and reference wafers are seed layers.

12. A machine accessible medium that provides instructions which, when executed by a processor, cause the processor to perform operations comprising:

measuring a first electrochemical deposition cell voltage of a reference wafer;

calculating a reference resistance using the first electrochemical deposition cell voltage of the reference wafer;

measuring a second electrochemical deposition cell voltage of a calibration wafer;

calculating a calibration resistance using the second electrochemical deposition cell voltage of the calibration wafer; and

comparing the reference resistance with the calibration resistance.

13. The machine accessible medium of claim 12, that causes the processor to perform operations further comprising:

measuring a first plurality of electrochemical deposition cell voltages of the reference wafer at a corresponding first plurality of electrochemical deposition currents; and

measuring a second plurality of electrochemical deposition cell voltages of the calibration wafer at a corresponding second plurality of electrochemical deposition currents.

14. The machine accessible medium of claim 12, that causes the processor to perform operations further comprising monitoring a electrochemical deposition of one or more production wafers using a selecting error trigger value.

15. The machine accessible medium of claim 14, that causes the processor to perform operations further comprising:

measuring the electrochemical deposition cell voltages of the one or more production wafers; and

determining when one of the electrochemical deposition cell voltages of the one or more production wafers is approximately equal to or greater than the edge trigger value.

16. The machine accessible medium of claim 15, wherein the error trigger value is selected to be approximately a 25% difference from the measured first electrochemical deposition cell voltage of the reference wafer.

17. A system, comprising:

an electroplater; and

a computer coupled to the electroplater, the computer comprising:

a processor; and

a memory to store instructions which, when executed by the processor, cause the processor to perform operations comprising:

measuring a first plating cell voltage of a reference wafer;

calculating a reference resistance using the first plating cell voltage of the reference wafer;

measuring a second plating cell voltage of a calibration wafer;

calculating a calibration resistance using the second plating cell voltage of the calibration wafer; and

comparing the reference resistance with the calibration resistance.

18. The system of claim 17, the memory to further store instructions which, when executed by the processor, cause the processor to perform operations further comprising:

measuring a first plurality of plating cell voltages of the reference wafer at a corresponding first plurality of plating currents; and

measuring a second plurality of plating cell voltages of the calibration wafer at a corresponding second plurality of plating currents.

19. The system of claim 18, the memory to further store instructions which, when executed by the processor, cause the processor to perform operations further comprising monitoring a plating of one or more production wafers using a selecting error trigger value.

20. The system of claim 19, the memory to further store instructions which, when executed by the processor, cause the processor to perform operations further comprising:

measuring the plating cell voltages of the one or more production wafers; and

determining when one of the plating cell voltages of the one or more production wafers is approximately equal to or greater than the edge trigger value.

21. The system of claim 20, wherein the error trigger value is selected to be approximately a 25% difference from the measured first plating cell voltage of the reference wafer.